REMARKS

Claim 25 has been amended. Attached hereto is a marked-up version of the changes made to the claim by the current amendment. The attached page is captioned "Version with markings to show changes made." Claims 25-30 are pending.

Claims 25-27 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Gardner (U.S. Patent No. 5,899,721). Claim 28-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gardner in view of Bai (U.S. Patent No. 5,861,340). Claim 30 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Gardner. These rejections are respectfully traversed.

The present invention is directed at a semiconductor device. Referring to Figs. 4-9 the semiconductor device of the present invention includes a gate electrode stack 10 disposed upon a dielectric film 16 over a portion of a wafer, such as substrate 17. The gate stack 10 includes a plurality of layers, for example, layers 11, 12, 13, 14, and 15. Above the gate stack 10 is an oxide cap 20. In one embodiment, the electrode stack 10 includes a polysilicon layer 11 and at least one metal layer 13. As shown in the figures, the sidewalls 18 of the electrode stack are continuously vertical. Surrounding the sidewalls 18, continuously from the bottom to the top of the sidewalls 18 are composite spacers, each of which comprise a nitride spacer 22 stacked above an oxide spacer 20. As illustrated, the nitride spacer 22 portion of each composite spacer extends along most of the the continuously vertical sidewalls 18, except for the bottom portion. The oxide spacer 22 portion of the composite spacer extends along the bottommost portion of the sidewalls 18.

Gardner is directed at a method of forming small spacers, as illustrated by Fig. 9. Gardner teaches a semiconductor device including a stack, which is comprised of a gate oxide (Fig. 9, layer located immediately under 104), a polysilicon gate conductor 104, and a metal silicide 122. Figs. 3-9 illustrate the method of Gardner constructing the semiconductor device. Significantly, as illustrated by Fig. 7, Gardner's composite spacer, which comprises a nitride portion 114 and an oxide portion 116, is formed before the stack is fully formed. Indeed, Fig. 7 illustrates the composite spacers as running only along the sidewalls of the stack when the stack consists only of the gate oxide layer and the polysilicon gate conductor layer 104. The metal silicide layer 122 of the stack is not formed until the next step, which is illustrated by Fig. 8, to yield the completed gate stack shown in Fig. 9. As a result of this method of construction, the composite spacers in Gardner's device do not span from the bottom to the top of the sidewalls of the stack. As illustrated in Fig. 9, parts of the sidewall from the metal silicide layer 122 are not surrounded by the composite sidewall. Gardner therefore fails to disclose or suggest an integrated circuit having "a plurality of composite spacers each extending continuously from a bottom to a top of said continuously vertical sidewalls, wherein each of said composite spacers further comprises a nitride spacer vertically stacked above an oxide spacer" as required by independent claim 25.

Bai is cited by the Office Action for teaching a refractory silicide metal layer, a diffusion layer, and a barrier layer which is substantially impermeable to silicon and metal atoms. However, as illustrated in Fig. 2C, Bai also fails to teach a spacer which extends from the bottom to the top of a continuously vertical sidewall. Indeed, Bai's spacer is not

even a composite spacer.

Claim 25 recite an integrated circuit including "a plurality of composite spacers each extending continuously from a bottom to a top of said continuously vertical sidewalls, wherein each of said composite spacers further comprises a nitride spacer vertically stacked above an oxide spacer." The cited prior art is devoid of any teachings or suggestions of this feature. Claim 25 is therefore believed to be allowable over the prior art of record. Claims 26-30 depend from claim 25 and are believed to be allowable over the prior art of record for these reasons and because the combination defined in the claims is not shown or suggested by the cited references.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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Version With Markings to Show Changes Made

Please amend claim 25 as follows:

25. An integrated circuit comprising:

a semiconductor substrate;

a gate dielectric film disposed on a surface of the substrate;

a gate electrode stack disposed on the gate dielectric film, wherein the stack includes a plurality of layers forming continuously vertical sidewalls; and

a plurality of composite spacers each extending continuously from a bottom to a top of said continuously vertical sidewalls, wherein each of said composite spacers further comprises a nitride spacer vertically stacked above an oxide spacer.

[nitride spacers extending along the continuously vertical sidewalls of the gate electrode stack other than along lowermost portions of the continuously vertical sidewalls.]